IN THE SPECIFICATION:

On page 1 please replace [0001] paragraph with the following paragraph:

This is a continuation-in-part of U.S. patent application serial no. 09/802,678, filed March 9, 2001, which is a continuation-in-part of U.S. patent application serial no. 09/288,352, now U.S. patent no. 6,498,099, issued December 24, 2002, which is a continuation-in-part of U.S. patent application serial no. 09/095,803, now U.S. patent no. ~~6,299,200~~ 6,229,200, issued May 8, 2001.

On page 1 and 2, please replace [0004] paragraph with the following paragraph:

In order to overcome these and other disadvantages of the prior art, the Applicants previously developed a Leadless Plastic Chip Carrier (LPCC). According to Applicants' LPCC methodology, a leadframe strip is provided for supporting several hundred devices. Singulated IC dice are placed on the strip die attach pads using conventional die mount and epoxy techniques. After curing of the epoxy, the dice are wire bonded to the peripheral internal leads by gold (Au), copper (Cu), aluminum (Al) or doped aluminum wire bonding. The leadframe strip is then molded in plastic or resin using a modified mold wherein the bottom cavity is a flat plate. In the resulting molded package, the die pad and leadframe inner leads are exposed. By exposing the bottom of the die attach pad, mold delamination at the bottom of the die paddle is eliminated, thereby increasing the moisture sensitivity performance. Also, thermal performance of the IC package is improved by providing a direct thermal path from the exposed die attach pad to the motherboard. By exposing the leadframe inner leads, the requirement for mold locking features is eliminated and no external lead standoff is necessary, thereby increasing device density and reducing package thickness over prior art methodologies. The exposed inner leadframe leads function as solder pads for motherboard assembly such that less gold wire bonding is required as compared to prior art methodologies, thereby improving electrical performance in terms of board level parasitics and enhancing package design

flexibility over prior art packages (i.e. custom trim tools and form tools are not required). These and several other advantages of Applicants' own prior art LPCC process are discussed in Applicants' United States patent no. ~~6,299,200~~ 6,229,200, the contents of which are incorporated herein by reference.

On page 2 and 3, please replace [0006] paragraph with the following paragraph:

According to Applicants' U.S. patent no. 6,498,099, the contents of which are incorporated herein by reference, an etch back process is provided for the improved manufacture of the LPCC IC package. The leadframe strip is first subjected to a partial etch on one or both of the top and bottom surfaces in order to create a pattern of contact leads (pads) and a die attach pad (paddle). After wire bonding the contacts to a singulated semiconductor die, followed by overmolding and curing of the mold, the leadframe strip is exposed to a second full etch immersion for exposing the contact pads in an array pattern (i.e. multi-row) or perimeter pattern (i.e. single row), as well as the die attach pad. In the case of a package with multi-row I/O leads, this etch back step eliminates the requirement for two additional saw singulation operations (i.e. to sever the inner leads from the outer leads), and in both the single-row and multi-row configurations, the etch back step eliminates post mold processing steps (e.g. mold deflashing) and ensures superior device yield over the processing technique set forth in Applicants' United States patent no. ~~6,299,200~~ 6,229,200. Additionally, using this technique allows for higher I/O pad density and also allows for pad standoff from the package bottom which reduces stress in the solder joint during PCB temp cycling. Further, the technique allows for the use of a pre-singulation strip testing technique given that the electrical I/O pads are now isolated from

each other and testing in strip can take place. This feature greatly increased the handling and throughput of the test operation.

On page 3, please replace [0007] paragraph with the following paragraph:

In Applicant's co-pending U.S. application serial no. 09/802,678, Entitled Leadless Plastic Chip Carrier With Etch Back Pad Singulation, filed March 9, 2001, the contents of which are incorporated herein by reference, the etch-back LPCC process of Applicants' United States patent no. 6,498,099 is modified to provide additional design features. The leadframe strip is selectively covered with a thin layer photo-resist mask in predetermined areas. Following the application of the mask, an etch-barrier is deposited as the first layer of the contact pads and die attach pad, followed by several layers of metals which can include for example, Ni, Cu, Ni, Au, and Ag. This method of formation of the contact pads allows plating of the pads in a columnar shape and into a "mushroom cap" or rivet-shape as it flows over the photoresist mask. The shaped contact pads are thereby locked in the mold body, providing superior board mount reliability. Similarly, the die attach pad can be formed in an interlocking shape for improved alignment with the die. The photo-resist mask is then rinsed away and the semiconductor die is mounted to the die attach pad. This is followed by gold wire bonding between the semiconductor die and the peripheral contact pads and then molding as described in Applicant's United States patent no. ~~6,299,200~~ 6,229,200. The leadframe is then subjected to full immersion in an alkaline etchant that exposes a lower surface of an array of the contact pads, a power ring and the die attach pad, followed by singulation of the individual unit from the full leadframe array strip.